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In re Inter Partes Reexamination of:
Jayesh BHAKTA et al.

Examiner: Woo H. CHOI

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Art Unit: 3992

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For: MEMORY MODULE DECODER

RESPONSE/AMENDMENT

MS Inter Partes Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated October 14, 2011, for which a response was due on December 14, 2011, and for which a one-month extension of time to extend the time for response from December 14, 2011 to January 17, 2012 (the first business day after January 14, 2012) was requested and granted, please consider the following.

There are no amendments to the specification or drawings.

Claim amendments begin on page 1 and continue to page 45.

Status of all claims is provided at page 46.

Remarks/Arguments begin on page 47.

An explanation of support for the new claims added with this Amendment begins on page 59.

A certificate of service is provided at page 63.

TABLE OF CONTENTS

Page

CLAIM AMENDMENTS 1
STATUS OF CLAIMS 46
A. Original Claims (Claims 1-51) 46
B. Previously Added Claims (Claims 52-118) 46
C. Newly Added Claims (Claims 119-136) 46
REMARKS 46
I. Introduction 47
II. Summary of Amendments 47
A. Original Claims 1-51 47
B. Previously Added Claims 52-118 48
C. Newly Added Claims 119-136 49
III. Ground 6 49
A. Original Claims 49
B. Previously Added Claims 49
IV. Ground 9 50
V. Ground 11 51
VI. Ground 12 51
A. Original Claims 51
B. Claims 7, 26, 33 and 44 52
VII. Ground 13 54
A. Original Claims 54
B. Previously Added Claims 54
C. Claims 7, 26, 33 and 44 55
VIII. Grounds 14 and 15 55
IX. Ground 16 56
X. Ground 17 57
XI. Ground 18 57
XII. Response to Arguments 57
XIII. Notice of Copending Proceedings 58
XIV. Explanation of Support for Claim Changes 59

TABLE OF CONTENTS
(continued)

Page

XV. Conclusion 61

CLAIM AMENDMENTS

Please **cancel** claims 64-66, 94-108 and 112-118.

Please **enter** the following amendments and new claims.

1. (Amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control

signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals.

2. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the

first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

3. (Original) The memory module of claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

4. (Original) The memory module of claim 3, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.

5. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit receives and buffers a plurality of row/column address signals of the input control signals during a row access procedure and sends the buffered plurality of row/column

address signals to the plurality of DDR memory devices during a subsequent column access procedure.

6. (Original) The memory module of claim 1, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

7. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer

system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

8. (Original) The memory module of claim 1, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

9. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR

memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the register comprises a plurality of register devices.

10. (Original) The memory module of claim 1, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

11. (Original) The memory module of claim 10, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the

first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

12. (Original) The memory module of claim 1, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

13. (Original) The memory module of claim 12, wherein the first rank is spaced from the second rank and the third rank is spaced from the fourth rank.

14. (Original) The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the second memory density greater than the first memory density.

15. (Amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one

chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to a bank address signal of the set of input signals.

16. (Amended) [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the command signal is transmitted to only one DDR memory device at a time.

17. (Original) The memory module of claim 16, wherein the command signal comprises a read command signal.

18. (Original) The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

19. (Original) The memory module of claim 18, wherein the command signal comprises a refresh command signal.

20. (Original) The memory module of claim 18, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.

21. (Amended) [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

22. (Original) The memory module of claim 15, wherein the command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address bit, and the circuit is configured to store the row address bit during an activate command for a selected bank.

23. (Amended) [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals,

the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure and to transmit the stored input signal as an output signal of the set of output signals during a subsequent column access procedure.

24. (Original) The memory module of claim 15, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

25. (Original) The memory module of claim 15, wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices.

26. (Amended) [The memory module of claim 25] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices, and

wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

27. (Original) The memory module of claim 15, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

28. (Amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals.

29. (Original) The memory module of claim 28, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

30. (Amended) [The memory module of claim 29] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in

response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device, and

wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

31. (Original) The memory module of claim 28, wherein the set of input control signals comprises fewer chip-select signals than does the set of output control signals.

32. (Original) The memory module of claim 31, wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals.

33. (Amended) [The memory module of claim 28] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the register receives the bank address signals and the input command signal of the set of input control signals.

34. (Original) The memory module of claim 28, wherein the first number of ranks is four and the second number of ranks is two.

35. (Original) The memory module of claim 28, wherein the first number of ranks is two and the second number of ranks is one.

36. (Original) The memory module of claim 28, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.

37. (Original) The memory module of claim 28, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.

38. (Original) The memory module of claim 28, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.

39. (Amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank

address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to a bank address signal of the set of input signals.

40. (Original) The memory module of claim 39, wherein the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals and wherein the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals, wherein the memory module simulates a virtual memory module having the second number of DDR memory devices.

41. (Original) The memory module of claim 39, wherein the at least one integrated circuit element comprises one or more integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.

42. (Original) The memory module of claim 39, wherein the row address signals and the column address signals of the plurality of input signals are received and buffered by the register and are sent from the register to the plurality of DDR memory devices.

43. (Original) The memory module of claim 42, wherein the logic element receives the second number of chip-select signals.

44. (Amended) [The memory module of claim 43] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals,

command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein the row address signals and the column address signals of the plurality of input signals are received and buffered by the register and are sent from the register to the plurality of DDR memory devices,

wherein the logic element receives the second number of chip-select signals, and

wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals.

45. (Original) The memory module of claim 39, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

46. (Original) The memory module of claim 39, wherein the plurality of DDR memory devices is arranged as the first rank of DDR memory devices on the first side of the printed circuit board, the second rank of DDR memory devices on the first side of the printed circuit board, a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth rank of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the fourth rank spaced from the DDR memory devices of the third rank.

47. (Original) The memory module of claim 39, wherein the DDR memory devices of the second rank are spaced from the DDR memory devices of the first rank in a direction along the first side.

48. (Original) The memory module of claim 39, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in the first rank, the second rank, a third rank, and a fourth rank, the third rank and the fourth rank on the second side of the printed circuit board.

49. (Original) The memory module of claim 39, wherein the plurality of input signals corresponds to a first memory density, and the plurality of output signals corresponds to a second memory density, the second memory density greater than the first memory density.

50. (Original) The memory module of claim 39, wherein the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting a command signal to at least one DDR memory device of the selected at least one rank.

51. (Amended) [The memory module of claim 39] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer

system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein the at least one integrated circuit element is configured to store a signal of the plurality of input signals during a row access procedure and to transmit the stored signal as an output signal of the plurality of output signals during a column access procedure.

52. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set

of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

53. (New) The memory module of claim 52, wherein the register receives and buffers the bank address signals and transmits the buffered bank address signals to the plurality of DDR

memory devices, the phase-lock loop device transmitting clock signals to the plurality of DDR memory devices and to both the logic element and the register.

54. (New) The memory module of claim 53, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation, wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device.

55. (New) The memory module of claim 54, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

56. (New) The memory module of claim 54, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the

computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

57. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control

signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

58. (New) The memory module of claim 57, wherein the bank address signals of the set of input control signals are received by the logic element and received and buffered by the register, the register transmitting the buffered bank address signals to the plurality of DDR memory devices, and the generation of the first number of chip-select signals of the output control signals by the logic element is responsive at least in part to the bank address signals.

59. (New) The memory module of claim 58, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

60. (New) The memory module of claim 58, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

61. (New) The memory module of claim 1, wherein the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices.

62. (New) The memory module of claim 61, wherein the at least one attribute comprises the number of ranks of DDR memory devices and the memory density per rank.

63. (New) The memory module of claim 62, wherein the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

64-66. (Cancelled)

67. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer

system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

68. (New) The memory module of claim 67, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device, wherein the memory module is operable for use in a server system.

69. (New) The memory module of claim 67, wherein the memory module is operable to perform successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

70. (New) The memory module of claim 67, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

71. (New) The memory module of claim 67, wherein the bank address signals include bank address signals received during an activate command operation and bank address signals

received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation.

72. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to a first set of values of at least one address bit and the at least one chip-select signal of the set of input control signals by generating rank-selecting signals of the set of output control signals that select none of the first number of ranks for activation, and the logic element is further responsive at least in part to a second set of values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select two ranks of the first number of ranks for activation.

73. (New) The memory module of claim 72, wherein the logic element is further responsive at least in part to values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for activation, and the logic element is further responsive at least in part to the values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for read or write access.

74. (New) The memory module of claim 73, wherein the at least one address bit comprises a row address bit and a bank address bit.

75. (New) The memory module of claim 1, wherein each DDR memory device of the plurality of DDR memory devices is a DDR dynamic random-access memory (DRAM) chip package with a bit width, and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR

DRAM chip packages of the rank, wherein the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has.

76. (New) The memory module of claim 75, wherein the DDR DRAM chip packages are DDR2 chip packages, DDR3 chip packages, or chip packages beyond DDR3 chip packages.

77. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of

input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input signals by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals.

78. (New) The memory module of claim 77, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

79. (New) The memory module of claim 77, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device.

80. (New) The memory module of claim 15, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as

having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

81. (New) The memory module of claim 80, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

82. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output

command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the logic element is responsive at least in part to the bank address signals and the chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

83. (New) The memory module of claim 82, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR DRAM device boundaries.

84. (New) The memory module of claim 82, wherein the plurality of DDR DRAM devices and the logic element are timed to clock signals from the phase-lock loop device.

85. (New) The memory module of claim 28, wherein the plurality of DDR DRAM devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of bank address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank, the memory module further comprising a read-only

memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR DRAM devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR DRAM devices.

86. (New) The memory module of claim 85, wherein the one or more attributes comprise the number of ranks of DDR DRAM devices and the memory density per rank and the data characterizes the plurality of DDR DRAM devices as having fewer ranks of DDR DRAM devices than the plurality of DDR DRAM devices actually has, and as having a greater memory density per rank than the plurality of DDR DRAM devices actually has.

87. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first

number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein the logic element is responsive at least in part to the bank address signals and the second number of chip-select signals of the plurality of input signals by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the set of input signals.

88. (New) The memory module of claim 87, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

89. (New) The memory module of claim 87, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device.

90. (New) The memory module of claim 39, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-

only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

91. (New) The memory module of claim 90, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

92. (New) The memory module of claim 1, wherein the memory module receives row/column address bits (A_0 - A_{n+1}), and the DDR memory devices are responsive at least in part to row/column address bits (A_0 - A_n), wherein the logic element operates in response at least in part to row/column address bit A_{n+1} and does not operate in response to the row/column address bits (A_0-A_n), and the register operates in response at least in part to the row/column address bits (A_0 - A_n) and does not operate in response to the row/column address bit A_{n+1}.

93. (New) The memory module of claim 39, wherein the at least one integrated circuit element receives address bits (A_0 - A_{n+1}), and the DDR memory devices are responsive at least in part to address bits (A_0 - A_n), wherein the logic element operates in response at least in part to address bit A_{n+1} and does not operate in response to the address bits (A_0 - A_n), and the register operates in response at least in part to the address bits (A_0 - A_n) and does not operate in response to the address bit A_{n+1}.

94-108. (Cancelled)

109. (New) The memory module of claim 1, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

110. (New) The memory module of claim 28, wherein the memory module comprises means for characterizing the plurality of DDR DRAM devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

111. (New) The memory module of claim 39, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

112-118. (Cancelled)

119. (New) The memory module of claim 2, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

120. (New) The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the first memory density greater than the second memory density.

121. (New) The memory module of claim 1, wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

122. (New) The memory module of claim 1, wherein the register comprises a plurality of register devices.

123. (New) The memory module of claim 1, wherein the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

124. (New) The memory module of claim 123, wherein the register receives and buffers the bank address signals and transmits the buffered bank address signals to the plurality of DDR memory devices, the phase-lock loop device transmitting clock signals to the plurality of DDR memory devices and to both the logic element and the register.

125. (New) The memory module of claim 124, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation, wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device.

126. (New) The memory module of claim 125, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column

address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

127. (New) The memory module of claim 125, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

128. (New) The memory module of claim 1, wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

129. (New) The memory module of claim 128, wherein the bank address signals of the set of input control signals are received by the logic element and received and buffered by the register, the register transmitting the buffered bank address signals to the plurality of DDR memory

devices, and the generation of the first number of chip-select signals of the output control signals by the logic element is responsive at least in part to the bank address signals.

130. (New) The memory module of claim 129, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

131. (New) The memory module of claim 129, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

132. (New) The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.

133. (New) The memory module of claim 132, wherein the command signal comprises a read command signal.

134. (New) The memory module of claim 25, wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

135. (New) The memory module of claim 28, wherein the register receives the bank address signals and the input command signal of the set of input control signals.

136. (New) The memory module of claim 43, wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals.

STATUS OF CLAIMS

Pursuant to 37 C.F.R. §§ 1.530(e) and 1.941, and with entry of this Amendment, claims 1-63, 67-93, 109-111 and 119-136 are pending, with claims 64-66, 94-108 and 112-118 cancelled. The following sets forth in more detail the status of the claims, and an explanation of support for the changes is provided in Section XIV of the Remarks.

A. Original Claims (Claims 1-51)

In this Amendment, the Patent Owner amends original independent claim 1 to include the recitation of allowable claim 66. Original independent claims 15, 28 and 39 have been similarly amended. Original dependent claims 2, 5, 7, 9, 16, 21, 23, 26, 30, 33, 44 and 51 have been placed in independent form. The remaining original dependent claims are also pending.

B. Previously Added Claims (Claims 52-118)

Claims 52-118 were added in the previous response by the Patent Owner. In this Amendment, the Patent Owner places previously added claims 52, 57, 67, 72, 77, 82 and 87 in independent form. Claims 64-66, 94-108 and 112-118 have been cancelled. The remaining previously added claims are pending, with claims 92 and 93 amended.

C. Newly Added Claims (Claims 119-136)

In this Amendment, the Patent Owner adds new claims 119-136.

REMARKS

I. Introduction

In the present reexamination of U.S. Patent No. 7,619,912 B2 (the '912 Patent), the Examiner issued a non-final Office Action on October 4, 2011. This Office Action, however, was superseded by a new Office Action on October 14 to take into account the comments of one of the Requesters. In the October 14 Office Action, the Examiner confirmed certain original dependent claims and found that certain previously added claims recited allowable subject matter.

The '912 Patent is currently the subject of two co-pending litigations that have been stayed. In an effort to expedite the reexamination and to simplify the issues, the Patent Owner hereby amends the claims based on the Examiner's indication of confirmed claims or allowable claims, with a few exceptions as discussed below, cancels some previously added claims without prejudice and adds new claims 119-136. Neither the amendments nor these Remarks should be in any way construed that the Patent Owner agrees or acquiesces to any of the rejections in the October 14 Office Action.

II. Summary of Amendments

A. Original Claims 1-51

In the October 14 Office Action, the Examiner found claim 66 to recite allowable subject matter. (*See, e.g.*, October 14 Office Action at 84.) The Patent Owner amends original independent claim 1 to recite the subject matter of claim 66. Original independent claims 15, 28 and 39 have been similarly amended.

In addition, the Examiner confirmed original dependent claims 2, 5, 9, 16, 17, 21, 23, 30 and 51. The Patent Owner has placed these claims in independent form, with the exception of claim 17 as it depends from claim 16.

Original dependent claims 7, 26, 33 and 44 have also been placed in independent form. All of these claims stand rejected, which the Patent Owner respectfully traverses as discussed below.

The remaining original dependent claims depend from claims 1, 15, 28 or 39 and are not amended.

B. Previously Added Claims 52-118

Based on the allowance of claim 66, it is believed that claims 52, 67, 77, 82 and 87 should also be allowed as discussed in more detail below. The Patent Owner has placed each of these previously added dependent claims in independent form.

The Examiner found claims 57 and 72 to recite allowable subject matter. (*See*, *e.g.*, October 14 Office Action at 84.) The Patent Owner has placed claims 57 and 72 in independent form.

The remaining previously dependent claims depend from claims 1, 15, 28, 39, 52, 57, 67, 72, 77, 82 or 87 and are not amended, except for claims 92 and 93. Previously added dependent claim 92 has been amended to recite "wherein the memory modules receives" as opposed to "wherein the set of input control signals includes," while claim 93 has been amended to recite "wherein the at least one integrated circuit element receives."

Finally, previously added claims 64-66, 94-108 and 112-118 have been cancelled without prejudice.

C. Newly Added Claims 119-136

The Patent Owner submits new claims 119-136. These claims are added to replace some of the dependent claims that have been placed in independent form. All the newly added claims depend from claims 1, 15, 28 and 39 and thus are allowable.

III. Ground 6

In view of the above amendments, the Patent Owner will address each pending ground of rejection beginning with Ground 6.

A. Original Claims

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Amidi and JEDEC 21-C. (*See* October 14 Office Action at 18-20 and 22.) The Examiner did not adopt the rejection as to claim 66. (*Id.* at 31.) Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 6 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 10-14, 18-20, 22, 24, 25, 27, 29, 31, 32, 34, 36-38, 40-43 and 45-50 under Ground 6. The Patent Owner respectfully requests that the Examiner withdraw Ground 6 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

B. Previously Added Claims

The Examiner rejected claim 52 under Ground 6. (*Id.* at 25-26.) The Patent Owner notes that claim 52 recites "the logic element is responsive at least in part to . . . the bank address signals . . . by generating a first number of chip-select signals of the set of output control signals . . . ." The Examiner cited his analysis of claim 1 for meeting this recitation. (*Id.* at 25.) The analysis of claim

1, however, does not address any such recitation. Indeed, later in the October 14 Office Action, the Examiner expressly found that "Amidi does not disclose that CAS or chip-select signals are generated in response to bank address signals" with respect to claim 66. (*Id.* at 31.) The Patent Owner thus respectfully submits that claim 52 should have been allowed over Ground 6. Claim 52 has been placed in independent form.

The same conclusion applies to previously added claims 67, 77, 82 and 87 which have similar recitations as claim 52 with respect to the bank address signals. The Examiner cited his analysis of claim 52 for meeting the recitations of these claims. (*Id.* at 27-29.) The analysis of claim 52 which, in turn, refers to claim 1 is not sufficient as discussed above. The Patent Owner thus respectfully submits that claims 67, 77, 82 and 87 should have been allowed over Ground 6. These claims have been placed in independent form. Claims 68-71, 78, 79, 83, 84, 88 and 89 depend from claims 67, 77, 82 and 87 and are likewise patentable over Ground 6.

The Examiner further rejected previously added (and currently pending) claims 61-63, 75, 80, 81, 85, 86, 90, 91 and 109-111 under Ground 6. All these claims depend from claims 1, 15, 28 and 39. Accordingly, the Patent Owner respectfully requests that the Examiner withdraw Ground 6 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

IV. Ground 9

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Dell 1 and JEDEC 21-C. (*See* October 14 Office Action at 35-37 and 38.) Neither the Requesters nor the Examiner challenged claim 66 under Ground 9. Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 9 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 18-20, 22, 24, 25, 27, 29, 31, 32, 36-38, 41-43, 45 and 50 under Ground 9. The Patent Owner respectfully requests that the Examiner withdraw Ground 9 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

V. Ground 11

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Wong and JEDEC 21-C. (*See* October 14 Office Action at 42-45.) Neither the Requesters nor the Examiner challenged claim 66 under Ground 11. Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 11 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 18-20, 22, 24, 25, 27, 29, 31, 32, 36-38, 41, 42, 43, 45 and 50 under Ground 11. The Patent Owner respectfully requests that the Examiner withdraw Ground 11 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

VI. Ground 12

A. Original Claims

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Micron and Connolly. (*See* October 14 Office Action at 48-50 and 52.) The Examiner did not adopt the rejection as to claim 66. (*Id.* at 58.) Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 12 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 10, 11, 18-20, 22, 24, 25, 27, 29, 31, 32, 35-38, 41-43, 45 and 50 under Ground 12. The Patent Owner respectfully requests that the Examiner withdraw Ground 12 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

B. Claims 7, 26, 33 and 44

Original dependent claim 7 recites "wherein the bank address signals of the set of input control signals are received by both the logic element and the register." Claim 26 also recites the bank address signals being received by the logic element and the register: "wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system." Claim 33 recites "wherein the register receives the bank address signals and the input command signal of the set of input control signals" and claim 28, from which claim 33 depends, recites the logic element receiving bank address signals. Finally, claim 44 recites "wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals." In short, all four of these claims recite the register receiving bank address signals.

In the October 14 Office Action, the Examiner relied on Micron, particularly Fig. 4, for these claims. (*See* October 14 Office Action, at 51, 54 and 55.) The bottom of Fig. 4 of Micron discloses a single unit Register that is designated with U37 and U38 receiving 22 input signals. Because the Examiner relied on U37 and U38 as meeting the logic element and register limitations and both appear to receive 22 input signals, the Examiner concluded that the register also receives bank address signals as recited in claims 7, 26, 33 and 44. The Patent Owner respectfully disagrees.

Micron discloses that the U37 and U38 designations refer to the SSTV16859 type which is compatible with JEDEC standard JESD82. (*See, e.g.*, Micron at Table 12 ("Register Specifications SSTV 16859 devices or equivalent JESD82-4B . . . Detailed Information for this register is available in JEDEC Standard JESD82.").) The cited JEDEC standard in turn defines each such register as a 13-bit registered buffer. (*See, e.g.*, JEDEC 82-4B, at page 1 and Fig. 1.) Therefore, Fig. 4 of Micron in fact refers to U37 and U38 as a single 22-bit register, as it takes two SSTV16859 registered buffers to register the 22 input signals (RAS, CAS, CKE0-1, WE, A0-A12, BA0-1, S0-1). Because each SSTV16859 can only register a portion of the 22 designated input signals, and nowhere does Micron describe which signals are registered by U37 versus U38, then Micron fails to disclose which of the 22 input signals are received by the logic element (U37), and which signals are received by the register (U38) to meet the claim recitation that the register receives bank address signals.

Even if one were to use input signals designations of Registers 1 and 2 of JEDEC 21-C, as shown on page 4.20.4-18 and referenced in Ground 6, to correspond to Micron's U37 and U38 registers respectively, then (i) the logic element (U37) would receive A0, A10, S0, S1, CAS, RAS, BA0, BA1, and WE which are associated with Register 2, and (ii) the register (U38) would receive A1-A9, A11, A12, CKE0, and CKE1 which are associated with Register 1. It is very clear that the Examiner's combination still would not result in a register that receives the bank address signals as clearly required by claims 7, 26, 33 and 44.

Therefore, the Patent Owner respectfully requests that the Examiner withdraw the rejection as to claims 7, 26, 33 and 44 under Ground 12.

VII. Ground 13

A. Original Claims

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Micron and Amidi. (*See* October 14 Office Action at 60-62 and 64.) The Examiner did not adopt the rejection as to claim 66. (*Id.* at 74.) Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 13 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 10, 11, 18-20, 22, 24, 25, 27, 29, 31, 32, 34, 36-38, 41-43 and 45 under Ground 13. The Patent Owner respectfully requests that the Examiner withdraw Ground 13 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

B. Previously Added Claims

The Examiner rejected claim 52 under Ground 13. (*Id.* at 67.) The Patent Owner notes that claim 52 recites "the logic element is responsive at least in part to . . . the bank address signals . . . by generating a first number of chip-select signals of the set of output control signals . . . ." The Examiner cited his analysis of claim 1 for meeting this recitation. (*Id.* at 60 and 67.) The analysis of claim 1, however, does not address any such recitation. Indeed, later in the October 14 Office Action, the Examiner expressly found that "Amidi does not disclose that CAS or chip-select signals are generated in response to bank address signals" with respect to claim 66. (*Id.* at 74.) The Patent Owner thus respectfully submits that claim 52 should have been allowed over Ground 13. Claim 52 has been placed in independent form. Claim 53 depend from claim 52 and is likewise patentable over Ground 13.

The same conclusion applies to previously added claims 67, 77, 82 and 87 which have similar recitations as claim 52 with respect to the bank address signals. The Examiner cited his analysis of claim 52 for meeting the recitations of these claims. (*Id.* at 70-71.) The analysis of claim 52 which, in turn, refers to claim 1 is not sufficient as discussed above. The Patent Owner thus respectfully submits that claims 67, 77, 82 and 87 should have been allowed over Ground 13. These claims have been placed in independent form. Claims 68-71, 78, 79, 83, 84, 88 and 89 depend from claims 67, 77, 82 and 87 and are likewise patentable over Ground 13.

The Examiner further rejected previously added (and currently pending) claims 61-63, 75, 76, 80, 81, 85, 86, 90, 91 and 109-111 under Ground 13. All these claims depend from claims 1, 15, 28 and 39. Accordingly, the Patent Owner respectfully requests that the Examiner withdraw Ground 13 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

C. Claims 7, 26, 33 and 44

All four of these claims recite the register receiving bank address signals as discussed above. As with Ground 12, the Examiner again relied on Micron for disclosing this limitation in his analysis for Ground 13. (*See* October 14 Office Action at 63, 65 and 67.) Therefore, the Patent Owner respectfully requests that the Examiner withdraw the rejection as to claims 7, 26, 33 and 44 under Ground 13 for the reasons discussed above.

VIII. Grounds 14 and 15

The Examiner rejected previously added claims 92-101 and 115-118 under § 112, first paragraph, for lack of written description, and claims 115-118 additionally for lack of enablement. (*See* October 14 Office Action at 76-78.)

With respect to the rejection of claims 92 and 93, claim 92 has been amended to recite "wherein the memory module receives" while claim 93 has been amended to recite "wherein the at least one integrated circuit element receives." It is believed that these amendments overcome the Examiner's rejection under Ground 14.

With respect to the rejection of claims 94-101 and 115-118, the Patent Owner has cancelled these claims without prejudice in order to expedite the reexamination and to simplify the issues. Thus, the rejections are moot. For clarity of record, the Patent Owner believes that these claims are supported and enabled by the specification. For example, the specification specifically discloses generating chip-select signals in at least Example 1 (spanning Columns 14-17), Fig. 1A (illustrating generated chip-select signals) and at Col. 23, lines 18-24, which provides:

> In certain embodiments, the PLD 42 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 32, 34, 36, 38. In certain other embodiments, the PLD 42 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS.sub.0a, CS.sub.0b, CS.sub.1a, and CS.sub.1b) which are each transmitted to a corresponding one of the four ranks 32, 34, 36, 38.

Nothing in this response should be construed that the Patent Owner agrees or acquiesces to these rejections.

IX. Ground 16

The Examiner rejected previously added claims 116-118 under § 112, second paragraph. (*See* October 14 Office Action at 80.) These claims have been rejected without prejudice in order to expedite the reexamination and to simplify the issues. Thus, the rejection is moot.

X. Ground 17

The Examiner rejected previously added dependent claim 76 as being obvious in view of Amidi, JEDEC 21-C and Vogt. (*See* October 14 Office Action at 83.) Claim 76 depends from claim 1 as amended. Neither the Requesters nor the Examiner challenged claim 66 under Ground 17. Moreover, the Examiner found claim 66 to be allowable over Amidi and JEDEC 21-C, and Vogt was not cited for the deficiencies of Amidi and JEDEC 21-C as to the recitation of claim 66. Accordingly, the Patent Owner respectfully requests that the Examiner withdraw Ground 17 as to claim 76 for at least this reason.

For clarity of record, the Patent Owner does not concede that Vogt is prior art to the claimed invention or that Vogt is a printed publication.

XI. Ground 18

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Micron, Connolly and Dell 2. (*See* October 14 Office Action at 83.) Neither the Requesters nor the Examiner challenged claim 66 under Ground 18. Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 18 as to claims 1, 15, 28 and 39.

XII. Response to Arguments

In the October 14 Office Action, particularly at pages 85-92, the Examiner made a number of statements, such as relating to the state of the art. The Patent Owner does not agree or acquiesce to these statements, and nothing in this response should be construed as agreeing or acquiescing to them. In fact, for clarity of record, the decision to not directly address in this Response any specific points, whether due to a claim cancellation or otherwise, does not indicate that Patent Owner agrees

with or acquiesces to these specific points. The Patent Owner reserves its rights to seek or defend similar claims in related applications or patents, which may be in reexamination. Furthermore, the Patent Owner discusses above only some of the claim features of the '912 patent for the sake of brevity. These discussions should not be interpreted as Patent Owner asserting or acquiescing that the claims are not disclosed or rendered obvious because of only these features.

Finally, with respect to the secondary considerations analysis, the Examiner appears to require a nexus between the praise/acceptance and the "claimed features that are found to be obvious." (*See* October 14 Office Action at 85.) This is not the proper legal standard. Instead, what is required is a nexus between the merits of the claimed invention and the evidence of secondary considerations. (*See* MPEP 716.01(b).) In addition, "[t]o be pertinent to the issue of nonobviousness, the commercial success of devices falling within the claims of the patent must flow from the functions and advantages disclosed or inherent in the description in the specification." (*See* MPEP 716.03(b).) Here, at minimum, the claimed invention as a whole achieves the laudable properties provided by the HyperCloud product, as described in the previously submitted Lee and Lopes declarations.

XIII. Notice of Copending Proceedings

Pursuant to 37 C.F.R. § 1.985(a), the Patent Owner identifies the co-pending litigations styled *Netlist, Inc. v. Inphi Corporation*, Case No. CV-09-6900-DSF (RNBx), in the United States District Court for the Southern District of California, and *Google v. Netlist*, 4:08-cv-04144-SBA (CAND), in the Northern District of California. These actions were stayed on May 18, 2010 and January 11, 2011 pending the present reexaminations of three other related patents: U.S. Patent No. 7,289,386 being reexamined in reexaminations bearing control nos. 95/000,546 and 95/000,577

(*Google* litigation only); U.S. Patent No. 7,532,537 being reexamined in the reexamination bearing control no. 95/001,381 (*Inphi* litigation only); and U.S. Patent No. 7,636,274 being reexamined in the reexamination bearing control no. 95/001,337 (*Inphi* litigation only).

In addition, the '912 Patent is related to following patents and pending applications: U.S. Patent No. 7,864,627 being reexamined in the reexamination bearing control no. 95/001,758; four newly issued patents, *i.e.*, U.S. Patent Nos. 8,072,837; 8,081,535, 8,081,536; and 8,081,537, as well as U.S. Patent Nos. 7,286,436, 7,881,150 and 7,916,574; and pending applications 12/912,623, 13/287,042 and 13/287,081.

XIV. Explanation of Support for Claim Changes

With respect to the amendment to independent claims 1, 15, 28 and 39, support for the amendment can be found in the specification and drawings including, without limitation, at Col. 14, line 17 to Col. 19, line 53, Col. 22, lines 50-63, Col. 23, lines 6-25 and Figs. 3A and 3B.

With respect to claims 2, 5, 7, 9, 16, 21, 23, 26, 30, 33, 44, 51, 52, 57, 67, 72, 77, 82 and 87, all of these claims have placed into independent form. Thus, they have been changed by adding the recitations of independent claims 1, 15, 28 or 39 to them. The support for the recitations of the independent claims 1, 15, 28 and 39 can be found in the specification and drawings including, without limitation, at Col. 5, lines 6-36, Col. 6, lines 12-16 and 31-38, Col. 6, line 55 to Col. 7, line 34, Col. 7, lines 35 to Col. 9, line 21, Col. 11, line 43 to Col. 12, line 10, Col. 22, lines 15-63, Col. 23, lines 6-25, Col. 28, lines 25-32 and Figs. 1A, 1B, 3A, 3B, 11A and 11B.

With respect to claims 92 and 93, support for the changes to claims 92 and 93 can be found in the specification and drawings including, without limitation, at Col. 7, lines 39-41 and Figs. 1A and 1B.

The Patent Owner respectfully submits new claims 119-136 for consideration with this Amendment. Almost all of these claims are added to replace some of the dependent claims that have been placed in independent form. All the newly added claims depend from claims 1, 15, 28 and 39 and thus are allowable for at least the reasons set forth above.

Claim 119 is identical to original claim 3, but depends from claim 2. Support for claim 119 can be found in the specification and drawings including, without limitation, at Col. 6, line 55 to Col. 7, line 19 and Figs. 1A and 1B.

Claim 120 depends from claim 1. Support for this claim can be found in the specification and drawings including, without limitation, at Col. 10, lines 49-55 and Col. 12, lines 12-15.

Claims 121 and 122 correspond to original dependent claims 7 and 9, which have been placed in independent form. Support for claims 121 and 122 can be found in the specification and drawings including, without limitation, at Col. 7, lines 50-53 for claim 121, and at Col. 5, lines 36-37 for claim 122.

Claims 123-127 depend from claim 1. The newly added dependent claims correspond to previously added dependent claims 52-56, as claim 52 has been placed in independent form. Support for claims 123-127 can be found in the specification and drawings including, without limitation, at the citations to the specification and drawings set forth at pages 21-22 of the Patent Owner's July 5 Response for claims 52-56 respectively.

Claims 128-131 depend from claim 1. The newly added dependent claims correspond to previously added dependent claims 57-60, as claim 57 has been placed in independent form. Support for claims 128-131 can be found in the specification and drawings including, without

limitation, at the citations to the specification and drawings set forth at pages 22-23 of the Patent Owner's July 5 Response for claims 57-60 respectively.

Claims 132-134 depend from claim 15. The newly added dependent claims correspond to original dependent claims 16 and 26, which have been placed in independent form, and claim 17. Support for claims 132-134 can be found in the specification and drawings including, without limitation, at Col. 8, lines 50-54 for claim 132; Col. 8, lines 44-54 for claim 133; and Col. 7, lines 50-53 for claim 134.

Claim 135 depends from claim 28. The newly added dependent claim corresponds to original dependent claim 33, which had been placed in independent form. Support for claim 135 can be found in the specification and drawings including, without limitation, at Col. 21, lines 54-66 and Figs. 2A and 2B.

Claim 136 depends from claim 39. The newly added dependent claim corresponds to original dependent claim 44, which has been placed in independent form. Support for claims 136 can be found in the specification and drawings including, without limitation, at Col. 7, lines 50-53.

XV. Conclusion

For the above reasons, the Patent Owner respectfully submits that the pending claims should be confirmed or allowed.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, the Patent Owner petitions for any required relief, including extensions of time, and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. **635162800300.**

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Respectfully submitted,

By _____

Mehran Arjomand
Registration No.: 48,231
MORRISON & FOERSTER LLP
555 West Fifth Street, Suite 3500
Los Angeles, California 90013
(213) 892-5630